



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,170	12/04/2003	Raminda Udaya Madurawe		6747

33380 7590 06/23/2005

RAMINDA U. MADURawe
882 LOUISE DRIVE
SUNNYVALE, CA 94087

EXAMINER

LE, DON P

ART UNIT PAPER NUMBER

2819

DATE MAILED: 06/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary

Application No. 10/727,170		Applicant(s) MADURAWA, RAMINDA UDAYA	
Examiner Don P. Le		Art Unit 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 December 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☒ Claim(s) 23 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>12/4/03</u> . | 6) <input type="checkbox"/> Other: _____ |

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 10 recites, **“wherein the programmable means further comprises...”**

the limitation is not mention anywhere in claim 8 or 1. To expedite the prosecution of this case, it is assumed that applicant refers to the programming of the programmable switch.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-22 are rejected under 35 U.S.C. 102(a) as being anticipated by Sugibayashi et al. (US 6,515,511).
5. With respect to claim 1, figures 3-24 of Sugi discloses a programmable wire structure for an integrated circuit, comprising:

Art Unit: 2819

a programmable switch (transistor 34-36, figure 14A) coupling two nodes (39, 28), said switch having a first state that connects said two nodes, said switch having a second state that disconnects said two nodes; and

a configuration circuit (wiring circuit 38 carrying signal to control transistor) coupled to said programmable switch, said circuit comprising a means to program said switch between said first and second state; and

a first metal layer (30) fabricated above a silicon substrate layer, said switch and said configuration circuit fabricated substantially above said first metal layer (as shown in figure 14A, the transistor and configuration wire carrying signal to gate of transistor have to be above metal layer 30).

6. With respect to claim 2, figure 14A of Sugi discloses a second metal layer (40) is fabricated substantially above said switch and said configuration circuit.

7. With respect to claim 3, figure 14A of Sugi discloses at least one of said first (39) and second (28) nodes is coupled to a node (30) in said first metal.

8. With respect to claim 4, at least one of said first (39) and second (28) nodes is coupled to a node (40) in said second metal.

9. With respect to claim 5, Sugi teaches thin film transistor (see abstract).

10. With respect to claim 6, figure 14A of Sugi discloses at least one of said first (39) and second (28) nodes of said programmable switch further comprises a via structure (39), said via structure containing a seed metal, said seed metal facilitating a thermally activated phase change of at least one of said thin film materials to improve conduction of said connect state (metal connection as shown in figure 14A improves conduction).

11. With respect to claims 7 and 12, the apparatus of Sugi discloses thin film

Art Unit: 2819

transistors (see abstract).

12. With respect to claims 8, 9, 13, 14 and 22, Sugi discloses a memory element is selected from one of fuse links, anti-fuse capacitors, SRAM cells, DRAM cells, metal optional links, EPROM cells, EEPROM cells, flash cells, ferro-electric elements, electrochemical elements, optical elements and magnetic elements (see column 1, lines 33-40).

13. With respect to claims 10 and 16, figure 14A of Sugi discloses a pass-gate device (transistor includes elements 34-36), said pass-gate controlled by an output signal from said memory element (SRAM), said first state generated by an on pass-gate, and said second state generated by an off pass-gate; and a configuration access to program said memory data, said memory bit polarity generating an on and off control signal to select said state of pass-gate device.

14. With respect to claims 11 and 15, figure 14A of Sugi discloses a wire structure for an integrated circuit having two selectable methods of connecting wires, comprising:

a first selectable method comprising programmable switches (34-35), each said switch coupling a wire in a first set (to a wire in a second set, and said method providing a means to program a user defined interconnect pattern between said first and second set of wires;

and a second selectable method comprising permanent connections in lieu of said switches, said permanent connection pattern duplicating one of said user defined interconnect patterns (vias connection from 30 to 32).

15. With respect to claim 17, the apparatus of Sugi is an array of programmable cells on a substrate layer.

Art Unit: 2819

16. With respect to claim 18, the apparatus of Sugi discloses a semiconductor device for integrated circuits with two selectable manufacturing configurations, comprising:

a first module layer having an array of structured cells (bottom layer, figure 14A), said module layer having at least one layer of metal (30);

and a second module layer formed substantially above said first module layer comprising two selectable configurations, wherein: in a first selectable configuration a programmable interconnect structure (transistors includes elements 34-36) is formed to connect said structured cells, and in a second selectable configuration a customized interconnect structure (vias between 32 and 30) is formed to connect said structured cells.

17. With respect to claim 19, figure 14A of Sugi discloses a third module layer (40) formed substantially above said second module layer comprised of a plurality of metal layers, said metal layers providing conductive wires to complete interconnect and routing of said semiconductor device.

18. With respect to claim 20, figure 4 of Sugi discloses each said structured cell comprising inputs and outputs, said inputs and outputs formed in said first module layer; and a portion of said inputs and outputs requiring one of said selectable second modules to connect to each other.

19. With respect to claim 21, it is inherent in the apparatus of Sugi (programmable logic device) said first selectable configuration comprised of a plurality of programmable interconnect patterns, a unique said pattern programmed by a user; and said second selectable configuration comprised of an interconnect pattern duplicating said unique programmed pattern; and said array of structured cells comprising an interconnect pattern, said interconnect pattern identical with either of said selectable options.

Allowable Subject Matter

20. Claim 23 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

21. The following is an examiner's statement of reasons for allowance:

With respect to claim 23, the prior art does not teach fabricating hard wire controls to replicate a specific memory pattern, wherein replicating comprises: a logic zero memory output mapped to a hard wire disconnect; and a logic one memory output mapped to a hard wire connect.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P. Le whose telephone number is 571-272-1806.


The examiner can normally be reached on 7AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2819

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

2/22/2005

A handwritten signature in black ink, appearing to read 'Don Le', with a stylized flourish at the end.

DON LE
PRIMARY EXAMINER